

# 10 Synchronization of the BTS3012 Clock

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## About This Chapter

The BTS3012 supports three clock synchronization modes, namely, Abis clock, external reference clock, and internal free run clock. Note that only one mode can be used in one time. The extraction, assignment, and free run functions of the clock in the BTS3012 are performed by the clock module in the DTMU.

### [10.1 Synchronization of the BTS3012/BTS3012AE Abis Clock](#)

The BTS3012/BTS3012AE extracts 2 MHz clock signals on the Abis interface. After the 2 MHz clock signals are phase-locked and frequency-divided, they are transmitted to the boards and modules for reference.

### [10.2 Synchronization of the BTS3012/BTS3012AE External Reference Clock](#)

The BTS3012/BTS3012AE supports synchronization with the external 2 MHz reference clock. The external reference clock works similarly as the Abis clock. As a high-precision clock reference in the DTMU, the 2 MHz reference clock provides the BTS with various clock signals and frame numbers.

### [10.3 Synchronization of the BTS3012/BTS3012AE Internal Clock](#)

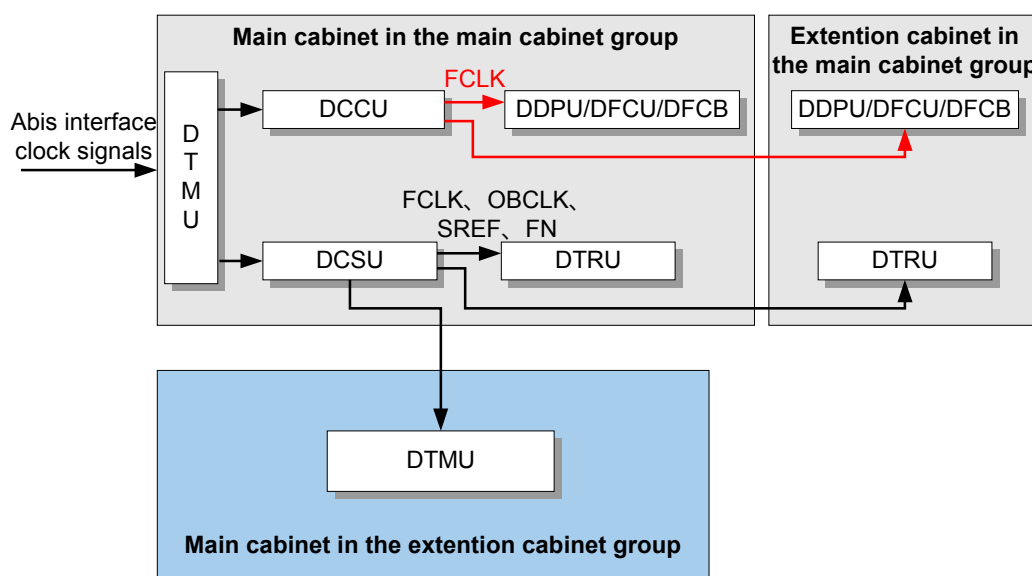
The BTS3012/BTS3012AE can use the internal reference clock. The internal reference clock guarantees the normal operation of the BTS when an external reference clock is unavailable.

## 10.1 Synchronization of the BTS3012/BTS3012AE Abis Clock

The BTS3012/BTS3012AE extracts 2 MHz clock signals on the Abis interface. After the 2 MHz clock signals are phase-locked and frequency-divided, they are transmitted to the boards and modules for reference.

**Figure 10-1** shows the processing and assigning of Abis clock signals.

**Figure 10-1** Processing and assigning of the Abis clock signals



### Procedure for Processing and Assigning the Clock Signals in the BTS Cabinet

The procedure for processing and assigning the clock signals in the main cabinet is as follows:

1. The DTMU extracts the 2 MHz clock signals through the Abis interface.
2. The clock signals are phase-locked and frequency-divided by the clock module of the DTMU before they are transmitted to the boards and modules for reference. The processed clock signals are categorized into frame clock (FCLK), frame number (FN), octet bit clock (OBCLK), and synchronizer reference (SREF) signals.
3. The DTMU assigns the clock signals (FCLK, OBCLK, SREF, and FN) to the boards and modules in the cabinet.
  - The DTMU assigns the clock signals to the DDPU, DFCU, or DFCB through the DCCU.
  - The DTMU assigns the clock signals to the DTRU through the DCSU.

### Procedure for Processing and Assigning the Clock Signals in the Combined Cabinets

The DTMU of the main cabinet assigns the clock signals (FCLK, OBCLK, SREF, and FN) to the boards and modules in the extension cabinet.

- The DTMU assigns the clock signals to the DDPU, DFCU, and DFCB of the extension cabinet through the DCCU.
- The DTMU assigns the clock signals to the DTRU of the extension cabinet through the DCCU.

## Procedure for Processing and Assigning the Clock Signals in the Cabinet Groups

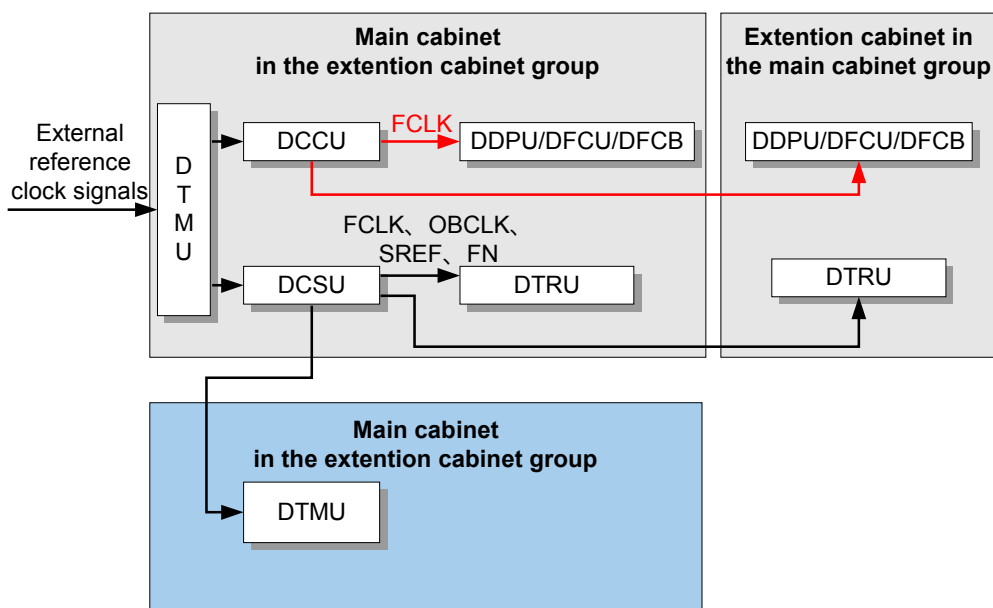
The DTMU in the main cabinet of the main cabinet group assigns the clock signals to the DTMUs in the main cabinets of the extension cabinet groups. Then, the DTMU in the main cabinet of the extension cabinet groups assigns clock signals for the boards and modules in the cabinets of the extension cabinet groups.

## 10.2 Synchronization of the BTS3012/BTS3012AE External Reference Clock

The BTS3012/BTS3012AE supports synchronization with the external 2 MHz reference clock. The external reference clock works similarly as the Abis clock. As a high-precision clock reference in the DTMU, the 2 MHz reference clock provides the BTS with various clock signals and frame numbers.

**Figure 10-2** shows the processing and assigning of the external reference clock.

**Figure 10-2** Processing and assigning of the external reference clock



## Procedure for Processing and Assigning the Clock Signals in the BTS Cabinet

The procedure for processing and assigning the clock signals in the main cabinet is as follows:

1. The DTMU in the main cabinet receives external reference clock signals with clock frequency as 2 MHz.
2. The clock signals are phase-locked and frequency-divided by the clock module of the DTMU before they are transmitted to the boards and modules for reference. The processed

clock signals are categorized into frame clock (FCLK), frame number (FN), octet bit clock (OBCLK), and synchronizer reference (SREF) signals.

3. The DTMU assigns the clock signals (FCLK, OBCLK, SREF, and FN) to the boards and modules in the cabinet.
  - The DTMU assigns the clock signals to the DDPU, DFCU, or DFCB through the DCCU.
  - The DTMU assigns the clock signals to the DTRU through the DCSU.

## Procedure for Processing and Assigning the Clock Signals in the Combined Cabinets

The DTMU of the main cabinet assigns the clock signals (FCLK, OBCLK, SREF, and FN) to the boards and modules in the extension cabinet.

- The DTMU assigns the clock signals to the DDPU, DFCU, and DFCB of the extension cabinet through the DCCU.
- The DTMU assigns the clock signals to the DTRU of the extension cabinet through the DCCU.

## Procedure for Processing and Assigning the Clock Signals in the Cabinet Groups

The DTMU in the main cabinet of the main cabinet group assigns the clock signals to the DTMUs in the main cabinets of the extension cabinet groups. Then, the DTMU in the main cabinet of the extension cabinet groups assigns clock signals for the boards and modules in the cabinets of the extension cabinet groups.

# 10.3 Synchronization of the BTS3012/BTS3012AE Internal Clock

The BTS3012/BTS3012AE can use the internal reference clock. The internal reference clock guarantees the normal operation of the BTS when an external reference clock is unavailable.

The internal reference clock of the BTS3012/BTS3012AE is integrated into the DTMU. It uses constant-temperature crystal oscillator to achieve high stability and performance. The clock frequency is 13 MHz. The combination of advanced algorithms and software phase-lock technique ensures the high precision of the internal reference clock.

**Figure 10-3** shows the processing and assigning of the internal reference clock.

Figure 10-3 Processing and assigning of the internal reference clock

